TRANSMITTAL OF APPEAL BRIEF	Docket No. M4065.0993/P993

In re Application of: Peter P. Altice, Jr.

Application No.	Filing Date	Examiner	Group Art Unit
10/751,440-Conf. #2571	January 6, 2004	C. W. A	2622

Invention: IMAGER DEVICE WITH DUAL STORAGE NODES

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: May 27, 2008 .

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Dated: September 22, 2008

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Docket No.: M4065.0993/P993
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Peter Parker Altice Jr.

Application No.: 10/751,440 Confirmation No.: 2571

Filed: January 6, 2004 Art Unit: 2622

For: IMAGER DEVICE WITH DUAL STORAGE NODES Examiner: C. W. A. CHEN

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This brief is filed within one month from the Notice of Panel Decision from Pre-Appeal Brief Review mailed on August 21, 2008.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I.	Real Party In Interest
II	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Claimed Subject Matter
VI.	Grounds of Rejection to be Reviewed on Appeal
VII.	Argument and Conclusion
VIII.	Claims Appendix
IX.	Evidence Appendix (none)
X.	Related Proceedings Appendix (none)

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is MICRON TECHNOLOGY, INC., the assignee of the application.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 45 claims pending in the application.

B. Current Status of Claims

1. Claims canceled: None

2. Claims withdrawn from consideration but not canceled: None

3. Claims pending: 1-45

4. Claims allowed: None

5. Claims rejected: 1-45

C. Claims On Appeal

The claims on appeal are claims 1-45

IV. STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the January 28, 2008 Final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed invention relates to a method and apparatus for an improved pixel cell for an imager which has an increased signal to noise ratio and increased charge storage capacity. (Present specification, Abstract). The pixel cell includes two storage nodes connected in parallel with each other and in series with a photodiode on one side and a floating diffusion region on the other. (Present specification, Abstract). The charge generated by the photodiode during a single integration period may be split up and stored on the two storage nodes and then is subsequently read out. (Present specification, paragraph [0009]). During applications requiring higher storage capacity, the entire charge from the photodiode over the single integration period may be captured on the two storage nodes, even when the charge is too large for a single storage node to capture. (Present specification, paragraph [0027]).

FIG. 3 from the present application is reproduced below as an example with which to better explain the claimed subject matter.

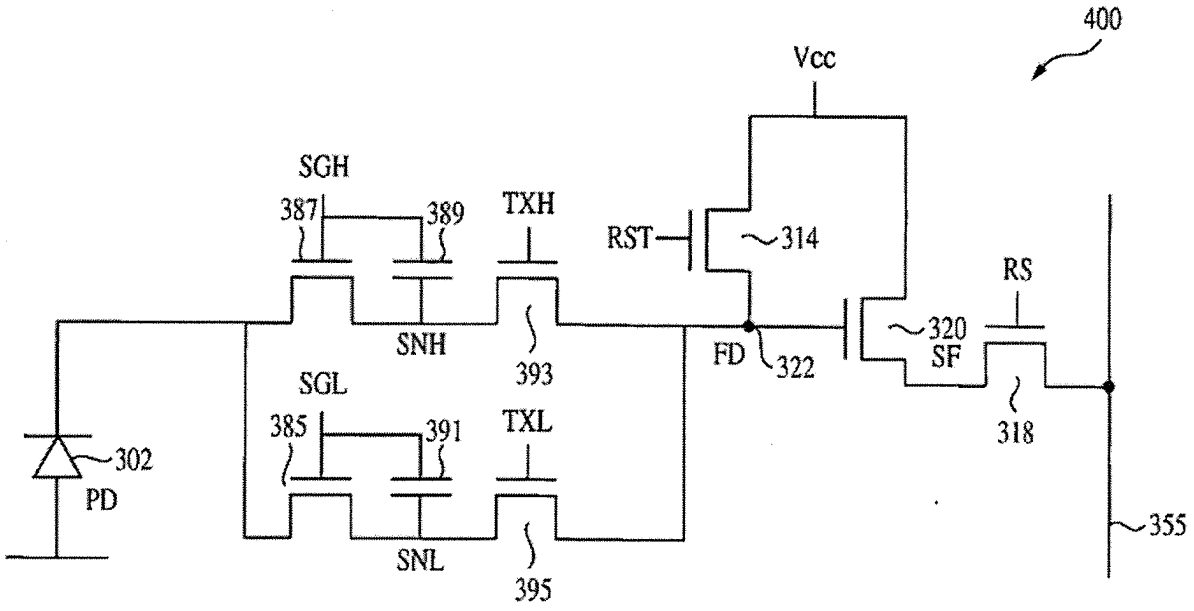

FIG. 3

Independent claim 1 is drawn to a pixel cell ("pixel cell 400") that includes a first storage node ("first storage node 389") for storing charge generated at a photosensitive element ("photodiode 302") during an integration period prior to storing the charge at a floating diffusion region ("floating diffusion region 322") of the pixel cell 400. (Present specification, paragraphs [0025]-[0026] and FIG. 3). The pixel cell 400 also includes a second storage node ("second storage node 391") for storing a portion of the charge generated by the photosensitive element 302 during the integration period that is not stored by the first storage node 389 and prior to storing the portion of the charge at the floating diffusion region 322. (Present specification, paragraphs [0025]-[0026] and FIG. 3).

It should be noted that claim 1 only refers to one integration period (i.e., "an integration period…the integration period"). Therefore, as recited by claim 1, the charge stored by both the

first storage node 389 and second storage node 391 is charge generated by the photosensitive element 302 during the same integration period. An integration period ends and the next integration period begins when the photosensitive element 302 is reset. (Present specification, paragraph [0031]). By storing charge from one photosensitive element 302 captured during one integration period on both the first storage node 389 and second storage node 391, the pixel cell 400 provides a larger charge storage capacity and an increased signal to noise ratio for a single integration period than a pixel cell using only one storage node per integration period or having no storage node at all. (Present specification, Abstract and paragraph [0007]).

Independent claim 11 is drawn to a semiconductor chip ("semiconductor chip 700") that includes a plurality of pixels cells having claimed features similar to those of the pixel cell of claim 1. (Present specification, paragraph [0039] and FIG. 7).

Independent claim 24 is drawn to a semiconductor chip ("semiconductor chip 800") including a plurality of pixel cells, where at least two of the pixel cells share a common floating diffusion node ("common floating diffusion region 322") and also have claimed features similar to those of the pixel cell of claim 1. (Present specification, paragraph [0040] and FIG. 8).

Independent claim 36 is drawn to a processor system ("processor based system 1200") including a processor ("central processing unit (CPU) 1202") and an imager device ("imager device 1208") including a plurality of pixel cells having claimed features similar to those of the pixel cell of claim 1. (Present specification, paragraph [0046] and FIG. 12).

Independent claim 25 is drawn to a method for operating an image sensor. The method includes receiving, at a first storage node ("first storage node 389") of a pixel cell ("pixel cell 400"), charge generated by a photosensitive element ("photodiode 302") of the pixel cell 400 during an integration period. (Present specification, paragraphs [0025]-[0027] and FIG. 3). The method also includes receiving, at a second storage node ("second storage node 391") of the pixel cell 400, a portion of the charge generated by the photosensitive element 302 during the integration period not stored at the first storage node 389. (Present specification, paragraphs [0025]-[0027] and FIG. 3). The method also includes transferring the charge from at least one of the first 389 and second

storage nodes 391 to a floating diffusion region ("floating diffusion region 322") of the pixel cell 400. (Present specification, paragraphs [0025]-[0027] and FIG. 3).

Independent claim 33 is drawn to a method for operating an image sensor. The method includes receiving light at a photosensitive element ("photodiode 302") of a first pixel cell ("pixel cell 400") during an integration period and transferring charge generated during the integration period by the photosensitive element 302 to a first storage node ("first storage node 389") of the first pixel cell 400. (Present specification, paragraphs [0025]-[0027] and FIG. 3). The method also includes transferring a portion of the charge generated during the integration period not transferred to the first storage node 389 to a second storage node ("second storage node 391") of the first pixel cell 400. (Present specification, paragraphs [0025]-[0027] and FIG. 3). The method also includes transferring the charge from the first storage node 389 to a floating diffusion region ("floating diffusion region 322") of the first pixel cell 400, reading out the charge from the floating diffusion region 322, transferring the charge from the second storage node 391 to the floating diffusion region 322, and reading out the charge from the floating diffusion region 322. (Present specification, paragraphs [0025]-[0027] and FIG. 3).

It should be noted that claims 25 and 33, like claims 1, 11, 24 and 36, only refer to <u>one</u> integration period (i.e., "an integration period...the integration period"). That is, the charge transferred to the first storage node 389 and second storage node 391 is charge generated during <u>the same integration period</u>.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on appeal are:

A. The rejection of claims 1, 2, 4, 6, 9, 10-12, 14, 16, 19, 20-25, and 27-35 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 7,286,174 issued to Weale et al. ("Weale") in view of U.S. Patent Nos. 6,710,804 ("Guidash '804") or 6,160,281 ("Guidash '281").

B. The rejection of claims 3, 5, 7, 8, 13, 15, 17, 18, and 26 under 35 U.S.C. § 103(a) as being unpatentable over Weale in view of Guidash '804 and U.S. Patent No. 6,069,376 issued to Merrill ("Merrill").

C. The rejection of claims 36, 37, 39, 41, 44, and 45 under 35 U.S.C. § 103(a) as being unpatentable over Weale in view of Guidash '804 and U.S. Patent Application Publication No. 2003/0090575 ("Miyamoto").

D. The rejection of claims 38, 40, 42, and 43 under 35 U.S.C. § 103(a) as being unpatentable over Weale in view of Guidash '804, Merrill, and Miyamoto.

VII. ARGUMENT

A. The rejection of claims 1, 2, 4, 6, 9, 10-12, 14, 16, 19, 20-25, and 27-35 should be reversed because the combination of Weale and Guidash does not teach or suggest all of the limitations of independent claims 1, 11, 24, 25, and 33.

As discussed above in the Summary of Claimed Subject Matter, independent claims 1, 11, 24, 25, 33, and 36 generally recite that charge collected by a photosensitive element during an integration period (i.e., one integration period) is either stored by, transferred to, or received by a first storage node and that charge from the integration period (i.e., the same single integration period) not stored by, transferred to, or received by the first storage node is stored by, transferred to, or received by a second storage node. The present specification teaches that one integration period ends and the next integration period begins when the photosensitive element 302 is reset. (Present specification, paragraph [0031]).

For example, claim 1 is drawn to a pixel cell that includes "a first storage node for storing charge generated at a photosensitive element during an integration period...and a second storage node for storing a portion of said charge generated by said photosensitive element during the integration period that is not stored by said first storage node". (emphasis added).

Claim 11 is drawn to a semiconductor chip that includes "a plurality of pixel cells... comprising...a first storage node for storing charge generated at a photosensitive element during an integration period...and a second storage node for storing a portion of said charge generated during the integration period by said photosensitive element that is not stored by said first storage node". (emphasis added).

Claim 14 is drawn to a semiconductor chip that includes "at least two pixel cells...comprising...a first storage node for storing charge generated at a photosensitive element during an integration period...and a second storage node for storing a portion of said charge generated by said photosensitive element during the integration period that is not stored by said first storage node". (emphasis added).

Claim 25 is drawn to a method for operating an image sensor that includes "receiving, at a first storage node of a pixel cell, charge generated by a photosensitive element of said pixel cell during an integration period...[and] receiving, at a second storage node of said pixel cell, a portion of said charge generated by said photosensitive element during the integration period not stored at said first storage node". (emphasis added).

Claim 33 is drawn to a method for operating an image sensor that includes "receiving light at a photosensitive element of a first pixel cell during an integration period; transferring charge generated during the integration period by said photosensitive element to a first storage node of said first pixel cell; [and] transferring a portion of said charge generated during the integration period not transferred to said first storage node to a second storage node of said first pixel cell". (emphasis added).

Claim 36 is drawn to a processor system that includes "an array of pixel cells, each pixel cell comprising: a first storage node for storing charge generated at a photosensitive element during an integration period prior to storing said charge at a floating diffusion region of said pixel cell; and a second storage node for storing a portion of said charge generated by said photosensitive element during the integration period that is not stored by said first storage node". (emphasis added).

Appellants respectfully submit that the Weale and Guidash combination does not teach or suggest this limitation because (as discussed below) the Weale and Guidash combination requires storing charge from a first integration period at a first storage node and storing charge from a second and different integration period at a second storage node.

Weale describes a pixel that includes a photo site 110, a first storage node 120 and a second storage node 140. (Weale, column 3, lines 42-46). Weale states that "the control circuitry [for the pixel] transfers a first collected signal from the photo site to the first storage node during a first period, transfers a second collected signal from the photo site to the second storage node during a second period that follows the first period, and then transfer[s] the first and second collected signals out of the pixel during a third period that follows the second period." (Weale, column 3, lines 46-53). Weale explicitly teaches that the first period and the second period are separate and distinct first and second integration periods. Furthermore, Weale defines an integration period in the same way as the present specification does, that is, one integration period ends and the next integration period begins when the photosite is reset. For example, as a method of operating the pixel, Weale teaches that:

> "First the AB gate is pulsed in such a way as to hard reset the photosite. Then, the TCK1 gate is pulsed to reset the photosite to the level of the transfer gate. Then, the integration is performed. After integration, the charge is transferred via TCK1 to storage node #1. The photosite is again hard reset via the AB gate, then soft reset across the TCK2 gate, then the second integration takes place, then the accumulated charge is transferred to the storage node #2." (Weale, column 12, lines 14-21).

That is, Weale explicitly teaches that the first integration period ends and the second integration periods begins by resetting the photosite and that the charge from the first integration period is stored on storage node #1, while the charge from the second integration period is stored on storage node #2.

Therefore, Weale does not teach that charge collected by a photosensitive element during a single integration period is either stored by, transferred to, or received by a first storage node and that charge from the same single integration period not stored by, transferred to, or received by the first storage node is stored by, transferred to, or received by a second storage node as recited by independent claims 1, 11, 24, 25, 33, and 36.

The examiner cites Guidash '804 and Guidash '281 only as disclosing a floating diffusion node and, therefore, Guidash '804 or Guidash '281 cannot cure the deficiencies of Weale. (Final Office Action of 1/28/08, page 3). Accordingly, the rejection of independent claims 1, 11, 24, 25, 33, and 36 should be reversed. The remaining claims 2, 4, 6, 9, 10, 12, 14, 16, 19, 20-23, 27-32, 34 and 35 depend from claims 1, 11, 24, 25, or 33, or 36 and their rejection should be reversed for the same reason.

In response to the above argument, the Examiner only states that "in the broadest sense...[the] image capture cycle of Weale [which includes two integration periods] is construed as the [one] 'integration period' taught in the instant application." (Advisory Action of May 15, 2008, page 2). Appellants submit that the examiner's construction is far too broad, because two integration periods cannot fairly be construed as one, especially where Weale and the present specification define an integration period in the same way.

Furthermore, it would not be obvious to collect charge from the same integration period on the first storage node 120 and the second storage node 140 of Weale because the purpose of the pixel of Weale is "to collect and store two or more frames worth of data [i.e., two or more integration periods from the pixel array] and then subsequently read these frames out at a subsequent point in time," which necessarily requires storing charge from a first integration period on a first storage node and charge from a second integration period on a second storage node.

(Weale, column 2, lines 24-26). Weale defines a "frame" as the light collected by an array of pixels during a single integration period. (Weale, column 1, lines 20-21, "a single frame (an array of pixels) is collected during an integration period").

Weale uses these two separately captured and stored integration periods for a variety of purposes, each of which require that a first integration period be stored on a first storage node 120 and a second integration period be stored on a second storage node 140. For example, Weale teaches imaging a scene illuminated by a strobe light by capturing and storing charge on storage site #1 during a first integration period during which the strobe is on, capturing and storing charge on storage site #2 during a second integration period during which the strobe is off, and comparing the two charges. (Weale, column 2, lines 27-40). In another example, Weale measures motion between "two closely spaced exposures" (i.e., integration periods) to generate an output signal for only the parts of the scene that change between the exposures. (Weale, column 3, lines 3-6). None of the applications contemplated by Weale can be accomplished by storing charge from the same integration period on two separate storage nodes.

B. The rejection of claims 3, 5, 7, 8, 13, 15, 17, 18, and 26 should be reversed because these claims depend from allowable independent claims 1, 11, or 25 and Merrill does not cure the deficiencies of the Weale and Guidash '804 combination.

Merrill, which has only been cited as allegedly teaching a gated storage node, does not cure the above-noted deficiencies of the Weale and Guidash '804 combination. (Final Office Action of 1/28/08, page 8). Accordingly, the rejection of claims 3, 5, 7, 8, 13, 15, 17, 18, and 26 should be reversed.

C. The rejection of claims 36, 37, 39, 41, 44, and 45 should be reversed because these claims depend from allowable independent claim 36 and Miyamoto does not cure the deficiencies of the Weale and Guidash '804 combination.

Miymoto, which has only been cited as allegedly teaching the use of a processor, does not cure the deficiencies of the Weale and Guidash '804 combination. (Final Office Action of

1/28/08, page 11). Accordingly, the rejection of claims 36, 37, 39, 41, 44, and 45 should be reversed.

D. The rejection of claims 38, 40, 42, and 43 should be reversed because these claims depend from allowable independent claim 36 and Merrill and Miyamoto do not cure the deficiencies of the Weale and Guidash '804 combination.

As discussed above, Merrill and Miyamoto do not cure the deficiencies of the Weale and Guidash '804 combination. Accordingly, the rejection of claims 38, 40, 42, and 43 should be reversed.

CONCLUSION

For each of the foregoing reasons, Appellants respectfully submits that the claimed subject matter is not unpatentable over the cited combination. Appellants respectfully requests the reversal of the final grounds of rejection.

Dated: September 22, 2008

Respectfully submitted,

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VIII. Claims appendix

Claims Involved in the Appeal of Application Serial No. 10/751,440

1. (Previously presented) A pixel cell, comprising:

a first storage node for storing charge generated at a photosensitive element during an integration period prior to storing said charge at a floating diffusion region of said pixel cell; and

a second storage node for storing a portion of said charge generated by said photosensitive element during the integration period that is not stored by said first storage node and prior to storing said portion of said charge at said floating diffusion region.

2. (Original) The pixel cell of claim 1, wherein said photosensitive element is a photodiode.

3. (Original) The pixel cell of claim 1, wherein said first storage node comprises a gated storage node.

4. (Original) The pixel cell of claim 1, wherein said first storage node comprises a storage capacitor.

5. (Original) The pixel cell of claim 1, wherein said second storage node comprises a gated storage node.

6. (Original) The pixel cell of claim 1, wherein said second storage node comprises a storage capacitor.

7. (Original) The pixel cell of claim 3, wherein said gated storage node comprises:

a depletion area between said photosensitive element and said floating diffusion region; and

a barrier region adjacent to said depletion area.

8. (Original) The pixel cell of claim 7, wherein said depletion area and said barrier region comprise oppositely doped silicon.

9. (Original) The pixel cell of claim 1 further comprising a first transfer transistor switchably coupled between at least one of said first and second storage nodes and said floating diffusion region.

10. (Original) The pixel cell of claim 1 further comprising:

a first transfer transistor switchably coupled between said first storage node and said floating diffusion region; and

a second transfer transistor switchably coupled between said second storage node and said floating diffusion region.

11. (Previously presented) A semiconductor chip, comprising:

a plurality of pixel cells, each of said plurality of pixel cells comprising:

a first storage node for storing charge generated at a photosensitive element during an integration period prior to storing said charge at a floating diffusion region of said pixel cell; and

a second storage node for storing a portion of said charge generated during the integration period by said photosensitive element that is not stored by said first storage node and prior to storing said portion of said charge at said floating diffusion region.

12. (Original) The chip of claim 11, wherein said photosensitive element is a photodiode.

13. (Original) The chip of claim 11, wherein said first storage node comprises a gated storage node.

14. (Original) The chip of claim 11, wherein said first storage node comprises a storage capacitor.

15. (Original) The chip of claim 11, wherein said second storage node comprises a gated storage node.

16. (Original) The chip of claim 11, wherein said second storage node comprises a storage capacitor.

17. (Original) The chip of claim 13, wherein said gated storage node comprises:

a depletion area between said photosensitive element and said floating diffusion region; and

a barrier region adjacent to said depletion area.

18. (Original) The chip of claim 17, wherein said depletion area and said barrier region comprise oppositely doped silicon.

19. (Original) The chip of claim 11 further comprising a first transfer transistor switchably coupled between at least one of said first and second storage nodes and said floating diffusion region.

20. (Original) The chip of claim 11 further comprising:

a first transfer transistor switchably coupled between said first storage node and said floating diffusion region; and

a second transfer transistor switchably coupled between said second storage node and said floating diffusion region.

21. (Original) The chip of claim 11 further comprising a sample and hold circuit for receiving said charge stored by said floating diffusion region.

22. (Original) The chip of claim 21, wherein said sample and hold circuit comprises at least four storage nodes, each respectively for storing a reset voltage and a signal voltage representing a charge stored by each of said first and second storage nodes.

23. (Original) The chip of claim 21, wherein said sample and hold circuit further comprises at least two storage nodes for respectively storing a reset voltage of said floating diffusion region and a signal voltage of at least one of said first and second storage nodes.

24. (Previously presented) A semiconductor chip, comprising:

a plurality of pixel cells, at least two of which share a common floating diffusion region, each of said at least two pixel cells further comprising:

a first storage node for storing charge generated at a photosensitive element during an integration period prior to storing said charge at said common floating diffusion region; and

a second storage node for storing a portion of said charge generated by said photosensitive element during the integration period that is not stored by said first storage node and prior to storing said portion of said charge at said floating diffusion region.

25. (Previously presented) A method for operating an image sensor, the method comprising:

receiving, at a first storage node of a pixel cell, charge generated by a photosensitive element of said pixel cell during an integration period;

receiving, at a second storage node of said pixel cell, a portion of said charge generated by said photosensitive element during the integration period not stored at said first storage node; and

transferring said charge from at least one of said first and second storage nodes to a floating diffusion region of said pixel cell.

26. (Original) The method of claim 25, wherein said first act of receiving comprises receiving said charge at a gated storage node of said pixel cell.

27. (Original) The method of claim 25, wherein said second act of receiving comprises receiving said portion of said charge at a storage capacitor of said pixel cell.

28. (Original) The method of claim 25, wherein said act of transferring comprises:

transferring said charge from said first storage node to said floating diffusion region; and

transferring said charge from said floating diffusion region to a column line associated with said pixel cell.

29. (Original) The method of claim 25, wherein said act of transferring comprises:

transferring said charge from said second storage node to said floating diffusion region; and

transferring said charge from said floating diffusion region to a column line associated with said pixel cell.

30. (Original) The method of claim 25, wherein said first act of receiving comprises activating a shutter gate transistor coupled between said first storage node and said photosensitive element.

31. (Original) The method of claim 25, wherein said second act of receiving comprises activating a shutter gate transistor coupled between said second storage node and said photosensitive element.

32. (Original) The method of claim 25, wherein said act of transferring comprises activating a transfer transistor coupled between at least one of said first and second storage nodes and said floating diffusion region.

33. (Previously presented) A method for operating an image sensor, the method comprising:

receiving light at a photosensitive element of a first pixel cell during an integration period;

transferring charge generated during the integration period by said photosensitive element to a first storage node of said first pixel cell;

transferring a portion of said charge generated during the integration period not transferred to said first storage node to a second storage node of said first pixel cell;

transferring said charge from said first storage node to a floating diffusion region of said first pixel cell;

reading out said charge from said floating diffusion region;

transferring said charge from said second storage node to said floating diffusion region; and

reading out said charge from said floating diffusion region.

34. (Original) The method of claim 33 further comprising the act of resetting at least one of said photosensitive element and said floating diffusion region.

35. (Original) The method of claim 33 further comprising:

receiving light at a second photosensitive element of a second pixel cell;

transferring charge generated by said second photosensitive element to a first storage node of said second pixel cell;

transferring a portion of said charge not transferred to said first storage node of said second pixel cell to a second storage node of said second pixel cell;

transferring said charge from said first storage node of said second pixel cell to said floating diffusion region, wherein said first and second pixel cells share said floating diffusion region;

reading out said charge from said floating diffusion region;

transferring said charge from said second storage node of said second pixel cell to said floating diffusion region; and

reading out said charge from said floating diffusion region.

36. (Previously presented) A processor system, comprising:

a processor; and

an imager device coupled to said processor, said imager device having an array of pixel cells, each pixel cell comprising:

a first storage node for storing charge generated at a photosensitive element during an integration period prior to storing said charge at a floating diffusion region of said pixel cell; and

a second storage node for storing a portion of said charge generated by said photosensitive element during the integration period that is not stored by said first storage node and prior to storing said portion of said charge at said floating diffusion region.

37. (Original) The processor system of claim 36, wherein said photosensitive element is a photodiode.

38. (Original) The processor system of claim 36, wherein said first storage node comprises a gated storage node.

39. (Original) The processor system of claim 36, wherein said first storage node comprises a storage capacitor.

40. (Original) The processor system of claim 36, wherein said second storage node comprises a gated storage node.

41. (Original) The processor system of claim 36, wherein said second storage node comprises a storage capacitor.

42. (Original) The processor system of claim 38, wherein said gated storage node comprises:

a depletion area between said photosensitive element and said floating diffusion region; and

a barrier region adjacent to said depletion area.

43. (Original) The processor system of claim 42, wherein said depletion area and said barrier region comprise oppositely doped silicon.

44. (Original) The processor system of claim 36, wherein each pixel cell further comprises a first transfer transistor switchably coupled between at least one of said first and second storage nodes and said floating diffusion region.

45. (Original) The processor system claim 36, wherein each pixel cell further comprises:

a first transfer transistor switchably coupled between said first storage node and said floating diffusion region; and

a second transfer transistor switchably coupled between said second storage node and said floating diffusion region.

IX. evidence APPENDIX

Evidence Involved in the Appeal of Application Serial No. 10/751,440

No evidence is being submitted.

X. related proceedings APPENDIX

Related Proceedings Involved in the Appeal of Application Serial No. 10/751,440

No related proceedings are referenced and therefore, no copies of decisions in related proceedings are provided.